Method of Forming Active and Isolation Areas with Split Active Patterning

U.S. Patent Application of:

<u>Jia Li</u>, Inventor

<u>SGS-Thomson Microelectronics, Inc.</u>, Assignee

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Robert Groover, REG.PAT.ATTY.

Background of the Invention

The present invention relates to integrated circuit isolation structures.

Background: Isolation Technologies

Adjacent elements on an integrated circuit must be electrically isolated from each other if they are to function independently. Therefore, it has long been recognized that the most basic elements of integrated circuit technology include not only active devices and interconnect, but also isolation.

The standard industry process for isolation of CMOS circuits has long been LOCOS ("LOCal Oxidation of Silicon"). In this process, a stack of silicon nitride and silicon oxide layers (or a stack of silicon nitride, polysilicon and oxide layers), is patterned to provide an oxidation barrier in locations where active devices are to be formed (i.e., the active regions). This stack is referred to as an "active stack." Silicon is exposed in locations where a field oxide is desired for isolation. A "channel-stop" implant is then performed, using dopants which will prevent parasitic transistors from turning on. In CMOS processes (including BiCMOS, CBCMOS, etc.), two channel-stop implants are often necessary, one for P-type regions and one for N-type regions. Thus, two mask steps (in addition to the active mask) are

normally required.[1]

The wafer is then placed in an oxidizing environment to grow a thick field oxide (typically at least several thousand Ångstroms)[2] on the exposed silicon areas. Silicon under the nitride will generally not be oxidized EXCEPT at the edge of the active stack, where lateral diffusion of oxygen under the active stack will cause a tapered shape, known as a "bird's beak," in the resulting structure.

Background: Alternatives to LOCOS

A problem with LOCOS is that the bird's beak costs a substantial amount of area. For many years there have therefore been substantial attempts to find an alternative to LOCOS. Many of the proposed alternative technologies also use localized oxidation, with modifications to reduce the width of the bird's beak.[3]

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[1]In some processes it may be possible to save a mask by using a blanket implant for one of these. Such modifications are referred to as "counterdoping," since in some locations one implants will have to counteract the other. (*See, e.g.*, U.S. Patent 4,613,885 to Haken, which is hereby incorporated by reference.)

[2]The thickness of the field oxide must be sufficient that conductors atop the field oxide cannot invert the silicon under the oxide (with "channel-stop" or other doping therein), to turn on parasitic transistors.

[3]One class of approach uses sacrificial polysilicon. *See, e.g.*, Matsunaga *et al.*, "Selective Polysilicon Oxidation Technology for Defect Free Isolation," 1980 IEDM 565ff, which is hereby incorporated by reference.

Other approaches use additional nitride to provide some lateral barrier to encroachment during the oxide growth step. *See* Kurosawa *et al.*, "A New Bird's-Beak Free Field Isolation Technology for VLSI Devices," 1981 IEDM 384ff, which
(continued...)

Difficulties of Conventional Mask Allocation

All conventional isolation process using localized oxidation have the following drawbacks as applied to modern technology:

1. If both n and p channel stop implants must be performed, then 3 masks will be needed: one for active, one for NMOS channel stop, and one for PMOS channel stop. Counterdoping may be able to eliminate one of these masks, but counterdoping imposes its own constraints.

2. The critical dimension (CD), or minimum geometry, cannot be optimized for the active areas in both N-well and P-well regions, due to the depth difference caused by typical well formation processes.

3. Unless the active stack is capable of blocking the channel stop implants, the photoresist on top of active stack must be hardened after active etch to survive the channel stop implant patterning to block the dopant. Critical dimension and slope of the photoresist must be sacrificed in order for the photoresist to survive second patterning. Channel stop patterning is also affected by the first layer of photoresist.

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[3](...continued)
is hereby incorporated by reference ("**BOX**" isolation or "Buried OXide isolation"); Chiu *et al.*, "The SWAMI - A Defect Free and Near-Zero Bird's-Beak Local Oxidation Process and Its Application in VLSI Technology," 1982 IEDM 224ff, which is hereby incorporated by reference ("**SWAMI**" or "SideWAll Masked Isolation"); Hui *et al.*, "Electrical Properties of MOS Devices Made With SILO Technology," 1982 IEDM 220ff, which is hereby incorporated by reference ("**SILO**" or "Sealed Interface Local Oxidation").

Summary of the Invention

The present invention provides a new technique for forming active and isolation areas, wherein the active areas in p regions and n regions are etched separately, using two separate patterning steps. Each of these two patterning steps not only patterns the oxidation barrier, but also patterns the respective channel stop implant (and optionally also a silicon recess etch).

Advantages of the new process include (but are not limited to) the following:

1. Two masks are needed instead of the three which would otherwise be required (unless counterdoping were used) if both n-type and p-type channel stop implants must be performed.

2. The critical dimensions of the active areas can be optimized separately in the n and p regions.

3. Even if the active stack is incapable of blocking channel stop implant, it is not necessary to pattern photoresist on top of photoresist. In fact, with the disclosed innovative process, the active stack's power of blocking implant dopant is no longer a factor in choosing the active stack. Thus, higher energies can be used for the channel-stop implant if desired, without the difficulties of photoresis-on-photoresist processing.

4. The depth of recess etching into silicon in n and p regions can be independently adjusted to achieve the best planarization.

It should also be noted that the two needed masks can be expressed as logical combinations of an "active" pattern with an N+ pattern and a P+ pattern, respectively. Thus the masks needed for

using the present invention, while different from the conventional masks, can readily be generated for all existing layouts.

Brief Description of the Drawing

The present invention will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

Figure 1 shows a cross-sectional view of a silicon wafer during the p channel stop implant, in a sample embodiment of the invention. (The dotted lines show the surface of silicon in an alternative embodiment, where the silicon has been recess etched.)

Figure 2 shows a cross-sectional view of a silicon wafer during the n channel stop implant, in a sample embodiment of the invention. (The dotted lines show the surface of silicon in an alternative embodiment, where the silicon has been recess etched.)

Description of the Preferred Embodiments

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

An example of the disclosed innovative process is as follows. (These steps are performed on a conventional silicon substrate, after the N-wells and/or P-wells have been conventionally formed to define n-type regions 102 and p-type regions 104.)

1. Deposit/grow active stack 110 (e.g. 800Å of nitride over 130Å of pad oxide).

2. Deposit and pattern photoresist 120A to expose the active stack 110 over the isolation areas 130A in the n-type regions 102. (The active areas in the n-type region, and the whole p-type region, remain covered with photoresist.)

3. Etch the exposed portions of the active stack 110, to expose silicon in the isolation areas in the n-type region.

4. **[optional]** Recess etch silicon 102 if so desired, *e.g.* to a depth of 2000Å.

5. Perform PMOS channel stop implant 150A (*e.g.* 3×10^{12} cm^{-2} of phosphorus at 60 keV).

(**Figure 1** shows a cross sectional view of the wafer at this stage of the process.)

6. Remove photoresist 120A and clean wafer.

7. Deposit and pattern photoresist 120B to expose the active stack over the isolation areas 130B in the p-type region. (The active areas 140 in the p-type region 104, and the whole n-type region 102, remain covered with photoresist 120B.)

8. Etch the exposed portions of the active stack 110, to expose silicon 104 in the isolation areas 130Bhe p-type region 104

9. **[optional]** Recess etch silicon 104 if so desired, *e.g.* to a depth of 2000Å.

10. Perform NMOS channel stop implant 150B (*e.g.* 2.5×10^{13} cm^{-2} of Boron at 100 keV).

(**Figure 2** shows a cross-sectional view of the wafer at this stage of the process.)

11. Remove all photoresist and clean wafer.

12. **[optional]** If desired, after recess etch, deposit nitride overall and perform anisotropic etchback, to form nitride sidewall on active stack 110, to reduce lateral encroachment during field oxide growth.

13. Grow field oxide (*e.g.* to 5000Å) and remove active stack.

This finishes the active/isolation formation process. Processing can then continue with conventional further steps to form active devices, contacts, and interconnects.

Note that steps 7 through 11 can be performed before steps 2 through 6, if desired.

The steps of etching the active stack 110 and silicon 102/104 are preferably performed with conventional anisotropic plasma or RIE etching. As will be readily recognized by those skilled in the art, the particular process recipes and etch chemistries used for etching the

active stack would be adjusted for the particular stack composition used. (For example, if the active stack includes an intermediate layer of polysilicon, then at least part of the active stack etch of step 3 should not be highly selective to silicon. For another example, if optional steps 4 and 9 are used, then a single etch step can be used to perform steps 3 and 4 together, using appropriate modulation of etchant species or using a nonselective anisotropic etch. For another example, of course the etches used do not have to 100% anisotropic, i.e. do not strictly have to achieve 100% vertical sidewalls.) In any case, the particular chemistries used are not particularly relevant to the present invention.

Further Modifications and Variations

It will be recognized by those skilled in the art that the innovative concepts disclosed in the present application can be applied in a wide variety of contexts. Moreover, the preferred implementation can be modified in a tremendous variety of ways. Accordingly, it should be understood that the modifications and variations suggested below and above are merely illustrative. These examples may help to show some of the scope of the inventive concepts, but these examples do not nearly exhaust the full scope of variations in the disclosed novel concepts.

For example, the presently preferred embodiment has been described in the context of a LOCOS process. However, the innovative ideas can also be combined with various approaches using sidewall nitride on the active stack, as discussed above. The innovative ideas can also be adapted, if desired, for combination with the various

modified-LOCOS processes which have been proposed,

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given.